AMENDMENTS TO THE CLAIMS:

The following listing of claims replaces all prior listings, and all prior versions, of claims in the application.

LISTING OF CLAIMS:

1. (Currently Amended) A method for correcting the direct current offset portion (DC offset) of a first signal comprising the steps of:

[[-]]phase shifting said first signal for obtaining a second ~~signal~~ signal,

[[-]]comparing said first signal and said second signal with an estimated DC ~~offset.~~offset,

adjusting the estimated DC offset if the first signal and the second signal are found to be on different amplitude sides of said estimated DC offset, wherein the estimated DC offset is increased if the second signal is higher than the estimated DC offset and is decreased if the second signal is lower than the estimated DC offset.

2. (Currently Amended) A method according to ~~claim 1 characterised in that~~claim 1, wherein said estimated DC offset is adjusted if the result of the comparison ~~is, that~~ is that said first signal and said second signal are on different amplitude sides of said estimated DC offset.

3. (Currently Amended) A method according to ~~claim 1 characterized in that~~ claim 1, wherein said estimated DC offset is kept constant if the result of the comparison ~~is, that~~is that said first signal and said second signal are both higher than or are both lower than ~~on the same side of~~ said estimated DC offset.

4. (Currently Amended) A method according to ~~claim 1 characterised in that~~claim 1, wherein said phase shifted second signal is obtained by low pass filtering said first signal.

5. (Currently Amended) A method according to ~~claim 1 characterised in that~~ ~~it~~claim 1, wherein the method is used for correcting the DC offset portion of a received and demodulated radio frequency signal.

6. (Currently Amended) A method according to ~~claim 5 characterised in that~~claim 5, wherein said demodulation is a demodulation for GFSK modulated signals.

7. (Currently Amended) A device for ~~adjusting~~ correcting the direct current offset portion (DC offset) of a first signal comprising:

[[-]] an input for connecting to a signal line for receiving said first signal,

[[-]] a phase shifting element connected to the input for producing a phase ~~shiftedsignal~~ shifted second signal,

[[-]] means for ~~adjusting said~~providing an estimated DC ~~offset~~ offset, wherein said estimated DC offset is adjusted if said phase shifted second signal is connected to ~~its~~ an input of said means and ~~holding~~ said estimated DC offset is held constant if said phase shifted second signal is disconnected from ~~its input.~~the input of said means,

[[-]] an output signal line connected to the output of said ~~said~~ means for ~~adjusting~~ providing said estimated DC ~~offset~~ offset,

[[-]] a decision circuit for deciding if said first signal and said phase shifted second signal are on different or same amplitude sides of said estimated DC offset, and

[[-]] a switch for connecting said phase shifted second signal to the input of said means ~~for adjusting said estimated DC offset~~ if said decision circuit decides that said first signal and said phase shifted ~~sigan~~ second signal are on different amplitude sides of said estimated DC offset and disconnecting said phase shifted ~~input~~ second signal from the input of said means ~~for adjusting said estimated DC offset~~ if the decision circuit decides that said first signal and said phase shifted second signal are on the same side of said estimated DC offset .

8. (Currently Amended) A device according to ~~claim 7 characterised in that~~claim 7, wherein said means for phase shifting said first signal is a low pass filter.

9. (Currently Amended) A device according to ~~claim 7 characteristed in that~~claim 7, wherein said means for ~~adjusting~~ providing said estimated DC-offset is a low pass filter.

10. (Currently Amended) A device according to ~~claim 7 characterised in that~~claim 7, wherein said decision circuit comprises:

a first comparator circuit and a second comparator circuit ~~with~~ each having an input signal ~~lines~~ line X and an input signal ~~lines~~ line Y and comparing input signals at the signal lines X and Y, ~~whereby~~ the input signal line X of the first comparator circuit is connected to ~~the~~ an output of said ~~means for~~ phase shifting ~~said signal~~element and the input signal line X of the second comparator circuit is connected to ~~the input~~ receive the first signal and the input signal lines Y of the first and second comparator circuits ~~are~~ are, respectively, connected to the output signal line; and an Exclusive-OR (XOR) gate comprising two input signal ~~lines and the~~lines, an output of said XOR gate controlling ~~the switch, whereby~~said switch and the outputs of the first and second comparator ~~circuit~~ circuits are connected to the input lines of said XOR gate.

11. (Previously Presented) A radio frequency receiver comprising a device for correcting the DC offset according to claim 7 implemented as an analog circuit as part of said receiver.

12. (Previously Presented) An electronic device comprising a device for correcting the DC offset according to claim 7 implemented as a digital hardwired logic.

13. (Previously Presented) A device according to claim 7 for correcting the DC offset of a received and demodulated radio frequency signal.

14. (Previously Presented) A transceiver comprising a device for correcting the DC offset according to claim 7.

15. (Previously Presented) A communication device comprising a device for correcting the DC offset according to claim 7.